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L4	6	(((((direct near3 memory near3 access) DMA) with (latch register))) same (FIFO with (state adj2 machine))) and CPU and (mux multiplex$2) and (DSP (signal adj2 processor))	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/02/16 14:50
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L15	0	14 and 710/1.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/02/16 15:05
L16	52	((((direct near3 memory near3 access) DMA) with (latch register))) same (FIFO with (state adj2 machine))	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/02/16 15:10

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Terms used
direct **near/3** **memory** **near/3** **access** or **DMA** **paragraph** **latch** or **register** **paragraph** **FIFO** **paragraph** **state** **near/2** **machine** ar

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1 A decade of reconfigurable computing: a visionary retrospective
R. Hartenstein
March 2001 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: 📄 pdf(766.00 KB)   Additional Information: full citation, references, citings, index terms

2 Coarse grain reconfigurable architecture (embedded tutorial)
Reiner Hartenstein
January 2001   **Proceedings of the 2001 conference on Asia South Pacific design automation**

Full text available: 📄 pdf(167.05 KB)   Additional Information: full citation, abstract, references, cit

The paper gives a brief survey over a decade of R&D on coarse grain reconfigurable hardware and related compil
reconfigurable computing.

3 Data and memory optimization techniques for embedded systems
P. R. Panda, F. Catthoor, N. D. Dutt, K. Danckaert, E. Brockmeyer, C. Kulkarni, A. Vandercappelle, P. G. Kjeldsberg
April 2001   **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 6 Issu

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We present a survey of the state-of-the-art techniques used in performing data and memory-related optimizatior
at the memory subsystem, and impact one or more out of three important cost metrics: area, performance, and
architecture-independent optimizations in the form of code transoformations. We next cover a broad spectrum of

Keywords: DRAM, SRAM, address generation, allocation, architecture exploration, code transformation, data cac
customization, memory power dissipation, register file, size estimation, survey

4 A parallel embedded-processor architecture for ATM reassembly
Richard F. Hobson, P. S. Wong
February 1999 **IEEE/ACM Transactions on Networking (TON)**, Volume 7 Issue 1

Full text available: 📄 pdf(331.21 KB)   Additional Information: full citation, references, citings, index terms

Keywords: ATM, embedded systems, medium access control, segmentation and reassembly

5 The use of a meta-assembler to design an M code interpreter on AMD2900 chips
Stanley Habib, Xue-Liang Yang
December 1981   **Proceedings of the 14th annual workshop on Microprogramming**

Full text available: pdf(960.39 KB)   Additional Information: full citation, abstract, references, in

There have been several machine designs using microprogrammed control which interpretively execute intermed
announced Modula language uses M code as an intermediate language This paper describes how an AM-DAM290(
M code. The microcontrol is microprogrammed using the standard AMD AM2900 microfunctions to execute the M

6 altPm: a strategy for integrating IP with ATM
Guru Parulkar, Douglas C. Schmidt, Jonathan S. Turner
October 1995   **ACM SIGCOMM Computer Communication Review , Proceedings of the conference on
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This paper describes research on new methods and architectures that enable the synergistic combination of IP ar
based on an ATM core and a set of tightly coupled general-purpose processors. This $a^{It}t^p m$ (pronounced "IP on AT
congestion control, routing, resource management, and packe ...

7 Experience Using Multiprocessor Systems—A Status Report
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André Meyer
July 1995   **ACM SIGCHI Bulletin**, Volume 27 Issue 3

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use of a pen or pencil as the primary means of interaction between a user and a machine, picking up the familiar
that will be analyzed and put into context with other emerging technologies and visions.Starting with a short hist

9 Using the Alfa-1 simulated processor for educational purposes
Gabriel A. Wainer, Sergio Daicz, Luis F. De Simoni, Demian Wassermann
December 2001   **Journal on Educational Resources in Computing (JERIC)**, Volume 1 Issue.4

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Alfa-1 is a simulated computer designed for computer organization courses. Alfa-1 and its accompanying toolkit a
extending existing components. The DEVS formalism is used to model individual components and to integrate the
a computer's architecture. We introduce Alfa-1 and the toolkit, show how to extend existing components, and de:

Keywords: DEVS formalism, modeling computer architectures, systems specification

10 Fast detection of communication patterns in distributed executions
Thomas Kunz, Michiel F. H. Seuren
November 1997   **Proceedings of the 1997 conference of the Centre for Advanced Studies on Collabora**

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